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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,789	03/24/2004	Robert A. Greene	49581/P042US/10315832	4254
29053	7590	04/26/2006	EXAMINER	
DALLAS OFFICE OF FULBRIGHT & JAWORSKI L.L.P.			PHAM, LONG	
2200 ROSS AVENUE			ART UNIT	
SUITE 2800			PAPER NUMBER	
DALLAS, TX 75201-2784			2814	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/807,789	<b>Applicant(s)</b> GREENE, ROBERT A.	
	<b>Examiner</b> Long Pham	<b>Art Unit</b> 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 February 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

### **DETAILED ACTION**

The petition to withdraw the restriction requirement has been treated as a request for reconsideration.

The restriction requirement has been withdrawn and an action on merits as follows:

#### ***Claim Objections***

Claim 28 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 20 and 28 are the same.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soldavini et al. (US patent 5,909,034) in combination with Kwark et al. (US publication 2005/0116013) and Cini et al. (US patent 5,165,590) and Cyr et al. (US publication 2005/0212604).

With respect to claim 1, Soldavini et al. teach an integrated circuit comprising of (see figs. 1-6 and associated text):

Internal circuitry;

Package having at least two pins (27,28,29,30);

A first carrier 44a communicatively coupling said internal circuitry with a first one 27 of said at least two pins, wherein said first carrier carries a polarity;

A second carriers 44b communicatively coupling said internal circuitry with said first one 27 of said at least two pins, wherein said second carrier carries a polarity;

A third carrier communicatively coupling said internal circuitry with a second one 30 of said at least two pins, wherein said third carrier carries a polarity; and

A fourth carrier communicatively coupling said internal circuitry with said second one 30 of said at least two pins, wherein said fourth carrier carries a polarity.

Soldavini et al. teach that the first and second carriers coupled to the first pin and third and fourth carriers coupled to second pin have polarity but fail to teach the carriers coupled to the same pin have opposite polarity.

Kwark et al. teach the coupling of carriers or bonding wires having opposite polarity reduces the effective impedance. See [0046].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to have carriers or bonding wires coupling to a pin having opposite polarity in the device of Soldavini et al. to achieve the above benefit.

With respect to claim 2, Soldavini et al. further teach the package encloses the internal circuitry. See fig. 4.

With respect to claim 3, Soldavini et al. further teach the at least two pins 27, 30 provide an interface for the internal circuitry to a component external to the integrated circuit. See fig. 4.

With respect to claim 4, Soldavini et al. further teach the first, second, third, and fourth carriers are bondwires. See fig. 4.

With respect to claims 5, 6, 7, 8, and 9, Soldavini et al. fail to teach the internal circuitry includes resonant frequency circuitry, a voltage controlled oscillator, a differential voltage controlled oscillator, or a resonant tank.

Cyr et al. teach employing a differential voltage controlled oscillator having a resonant or LC tank to form a system that is capable of wide-band tuning so as to service multiple frequency bands. See [0011] and [0125].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cyr et al into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

With respect to claims 10 and 11, the bonding wires of the Soldavini et al. inherently have inductance.

With respect to claims 12 and 14, Soldavini et al. further teach coupling pins together (through bonding wires and inside the internal circuitry see fig. 4) but fail to teach coupling the pins externally as required by claim 13.

Cini et al. teach coupling pins 5,6 externally to improve connections. See abstract and fig. 1.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cini et al. into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

With respect to claim 15, Soldavini et al. in combination with Kwark et al. implicitly teach the first, second, third, and fourth carriers are arranged in parallel interleaving polarities carried thereby. See the above.

With respect to claim 16, Soldavini et al. further teach that first, second, third and fourth carriers are neighbors. See fig. 4.

With respect to claim 17, Soldavini et al. further teach that first and second pins are neighbors in the package. See fig. 4.

Claims 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soldavini et al. (US patent 5,909,034) in combination with Kwark et al. (US publication 2005/0116013) and Cini et al. (US patent 5,165,590) and Cyr et al. (US publication 2005/0212604).

With respect to claims 32, 34, 35, and 36, Soldavini et al. teach a system comprising of (see figs. 1-6 and associated text):

Circuitry implemented in a package that provides a plurality of interface means 27,30 that are electrically coupled together (see fig. 4);

First coupling means 44a for communicatively coupling said circuitry to one 27 of said plurality of interface means, wherein said first coupling means carries a signal of a polarity;

Second coupling means 44b for communicatively coupling said circuitry to one 27 of said plurality of interface means, wherein said second coupling means carries a signal of a polarity.

Third coupling means for communicatively coupling said circuitry to one 30 of said plurality of interface means, wherein said third coupling means carries a signal of a polarity;

Fourth coupling means for communicatively coupling said circuitry to one 30 of said plurality of interface means, wherein said fourth coupling means carries a signal of a polarity.

Soldavini et al. teach that the first and second coupling means coupling the circuitry to one of the interface means and third and fourth coupling means coupling the circuitry to other one of the interface means have polarity but fail to teach the coupling means coupled to the same interface means have opposite polarity.

Kwark et al. teach the coupling means or bonding wires having opposite polarity reduces the effective impedance. See [0046].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Kwark et al. into the device of Soldavini et al. to achieve the above benefit.

Further with respect to claim 32, Soldavini et al. teach the circuitry comprises of internal circuits but fail to teach the circuitry comprises of resonant tank circuit.

Cyr et al. teach employing a differential voltage controlled oscillator having a resonant or LC tank to form a system that is capable of wide-band tuning so as to service multiple frequency bands. See [0011] and [0125].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cyr et al into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

With respect to claim 33, the first coupling means and the second coupling means or bonding wires of the Soldavini et al. inherently have inductance.

With respect to claim 38, Soldavini et al. further teach a board to which said package is electrically coupled, wherein said plurality of interface means are electrically couple together on said board (through bonding wires and inside the internal circuitry see fig. 4) but fail to teach said plurality of interface means are electrically coupled together externally as required by claim 37.

Cini et al. teach interface means or coupling pins 5,6 externally to improve connections. See abstract and fig. 1.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cini et al. into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

Claims 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soldavini et al. (US patent 5,909,034) in combination with Kwark et al. (US

publication 2005/0116013) and Cini et al. (US patent 5,165,590) and Cyr et al. (US publication 2005/0212604).

With respect to claim 39, Soldavini et al. teach a system comprising of (see figs. 1-6 and associated text):

Internal circuitry implemented in a package that provides a plurality of pins 27,30 (see fig. 4);

A first plurality of carriers 44a,44b communicatively coupling said internal circuitry to a first one 27 of said plurality of pins, wherein the first plurality of carriers inherently have inductance for said internal circuitry, and wherein at least one of said first plurality of carriers carries a signal of a polarity and at least one other of said first plurality of carriers carries a signal of a polarity;

A second plurality of carriers communicatively coupling said internal circuitry to a neighboring pin 27 of said first one of said plurality of pins, wherein said second plurality of carriers inherently have inductance for said internal circuitry, and wherein at least one of said second plurality of carriers carries a signal of a polarity and at least one other of said second plurality of carriers carries a signal of a polarity;

Soldavini et al. teach that the first plurality of carriers coupled to the first one of the plurality of pins and the second plurality of carriers coupled to neighboring pin of said first one of said plurality of pins have polarity but fail to teach the carriers coupled to the same pin have opposite polarity.

Kwark et al. teach the coupling of carriers or bonding wires having opposite polarity reduces the effective impedance. See [0046].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to have carriers or bonding wires coupling to a pin having opposite polarity in the device of Soldavini et al. to achieve the above benefit.



With respect to claim 39, Soldavini et al. in combination with Kwark et al. implicitly teach the first, second, third, and fourth carriers are arranged in parallel interleaving polarities carried thereby. See the above.

With respect to claim 40, Soldavini et al. further teach said plurality of pins each provide an interface for communicatively coupling a component to external to the package. See fig. 4.

With respect to claims 41 and 44, Soldavini et al. further teach internal component electrically couples the first pin and said neighboring pin together (see fig. 4) but fail to teach external component electrically couples the first pin and said neighboring pin together.

Cini et al. teach interface means or coupling pins 5,6 externally to improve connections. See abstract and fig. 1.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cini et al. into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

With respect to claim 43, the first and second pluralities of carriers or bonding wires of the Soldavini et al. inherently have inductance.

Further with respect to claim 42, Soldavini et al. teach the circuitry comprises of internal circuits but fail to teach the circuitry comprises of resonant tank circuit.

Cyr et al. teach employing a differential voltage controlled oscillator having a resonant or LC tank to form a system that is capable of wide-band tuning so as to service multiple frequency bands. See [0011] and [0125].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cyr et al into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

Claims 18-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soldavini et al. (US patent 5,909,034) in combination with Kwark et al. (US

publication 2005/0116013) and Cini et al. (US patent 5,165,590) and Cyr et al. (US publication 2005/0212604).

With respect to claims 18 and 24, Soldavini et al. teach a method comprising of (see figs. 1-6 and associated text):

Coupling a first carrier 44a from an internal circuitry of an integrated circuit to an electrically common interface 27 of the integrated circuits' package, wherein first carrier is arranged to carry signals of a polarity;

Coupling a second carrier 44b from said internal circuitry of an integrated circuit to said electrically common interface 27 of the integrated circuits' package, wherein second carrier is arranged to carry signals of a polarity;

Coupling a third carrier from said internal circuitry of an integrated circuit to said electrically common interface 27 or interface 30 (since 27 and 30 are internally and electrically connected) of the integrated circuits' package, wherein third carrier is arranged to carry signals of a polarity;

Coupling a fourth carrier from said internal circuitry of an integrated circuit to said electrically common interface 27 or interface 30 (since 27 and 30 are internally and electrically connected) of the integrated circuits' package, wherein fourth carrier is arranged to carry signals of a polarity;

Soldavini et al. teach that the first and second carriers are coupled to the common interface and have a polarity and third and fourth carriers are coupled to the common interface and have a polarity but fail to teach the carriers coupled to the common interface have opposite polarity.

Kwark et al. teach the coupling of carriers or bonding wires having opposite polarity reduces the effective impedance. See [0046].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to have carriers or bonding wires coupling to a common interface having opposite polarity in the device of Soldavini et al. to achieve the above benefit.

With respect to claim 19, Soldavini et al. further teach that the coupling of said first, second, and third carriers from the internal circuitry to the electrically common interface are done by first, second, and third bonding wires, respectively.

With respect to claim 21, Soldavini et al. further teach the electrically common interface comprises at least one pin 27. See fig. 4.

With respect to claim 22, Soldavini et al. further teach the electrically common interface comprises a plurality of pins 27,30 that are electrically coupled together. See fig. 4.

With respect to claim 23, Soldavini et al. further teach the electrically common interface comprises a plurality of pins 27,30 that are electrically coupled together but fail to teach the plurality of pins are coupled externally.

Cini et al. teach coupling pins 5,6 externally to improve connections. See abstract and fig. 1.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cini et al. into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

With respect to claim 25, Soldavini et al. further teach that said electrically common interfaces comprises two pins 27,30 that are electrically coupled together (since both pins 27,30 are connected to the same internal circuitry and coupling said first and second carriers 44a,44b to a first one 27 of said two pins 27,30 and coupling said third and fourth carriers to a second one 30 of said two pins 27,30. See fig. 4 and associated text.

With respect to claim 26, Soldavini et al. in combination with Kwark et al. implicitly teach the first, second, third, and fourth carriers are arranged to interleave the signal polarities carried thereby. See the above.

With respect to claim 27, Soldavini et al. in combination with Kwark et al. implicitly teach arranging said first, second, third, and fourth carriers such that the neighboring carriers of any given one of said first, second, third, and fourth carriers

carry signals of opposite polarity relative to the polarity of signals carriers by said given one. See above.

With respect to claims 20 and 28, The first, second, and third carriers of Soldavini et al. would inherently have inductance for internal circuitry.

With respect to claim 29, Soldavini et al. in combination with Kwark et al. implicitly teach arranging said first, second, and third carriers to interleave the signal polarity carried thereby. See above.

With respect to claims 30 or 31, Soldavini et al. fail to teach the internal circuitry includes an oscillator or resonant tank.

Cyr et al. teach employing a differential voltage controlled oscillator having a resonant or LC tank to form a system that is capable of wide-band tuning so as to service multiple frequency bands. See [0011] and[0125].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Cyr et al into the device of Soldavini et al. and Kwark et al. to achieve the above benefit.

### ***Response to Arguments***

Applicant's arguments filed 02/23/06 have been fully considered but they are not persuasive. See below.

In response to the applicant's arguments on pages 10-12 of the response dated 02/23/06, it is submitted that how Cini is being relied in the rejection is recited in the office action dated 12/13/05. Further, note that Cini is being relied on for teaching of coupling pins externally to improve connections. See the rejection.

In response to the applicant's arguments on page 14 of the response dated 02/23/06, it is submitted that the fact that the applicants have a different reason or advantage resulting from doing what the relied prior art suggested doing is not indicative or demonstrative of unobviousness. In Re Kronig 190 USPQ 425,428 (CCPA 1976); In Re Lintner 173 USPQ 560 (CCPA 1972). Further, it is submitted that the prior art motivation or advantage may be different that that of applicants

while still supporting a conclusion of obviousness. In *Re Wiseman* 201 USPQ 658 (CCPA); *Ex Parte Obiaya* 227 USPQ 58 (Bd. of App. 1985). In this particular case, kwark et al. teach bonding wires having opposite polarities to improve connections whereas Soldavini et al. teach bonding wires to reduce resistance.

In response to the applicant's arguments on page 17 of the response dated 02/23/06, it is submitted that since Soldavini et al. in combination with Kwark et al. teach system having an internal circuitry having reduced impedance, it would have been obvious to one in skilled in the art to include a resonant tank in the internal circuitry to produce a system having a resonant tank that has reduced impedance.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Primary Examiner

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LP